UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,553	12/26/2001	Llewellyn Yance	P21848	8319

7055 7590 11/03/2004

GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191

EXAMINER	
PARK, EDWARD K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,553	YANCE ET AL.	
	Examiner	Art Unit	
	Edward K. Park	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *1,5 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1, 5 and 8 objected to because of the following informalities: in line 3 of claim 1, the phrase "operation speed" should be clarified to read "the low speed operation mode." In claims 5 and 8, the word "operations" in line 3 of both claims should be clarified to read "the low speed operation mode." Line 15 of claim 5 and line 18 of claim 8 refer to "the second time period," which lacks antecedence; these instances should read "a second time period." Line 17 of claim 8 refers to "the stop operation mode," which lacks antecedence and should read "a stop operation mode." Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui (U.S. 6,763,478) in view of Arai (5,978,922).

5. With respect to claim 1, Bui discloses a method for controlling a microcomputer in a microcomputer system (page 2, column 3, lines 60-61) with a high speed operation mode and a low speed operation mode (page 2, column 3, lines 60-64) in which operation speed of the microcomputer is slower than that of the high speed operation mode, said microcomputer system including a clock operable in the high and the low speed operation mode (page 2, column 4, lines 65-67 and page 3, column 5, lines 1-2) and a backup power supply for supplying the clock with power for a predetermined time (page 2, column 3, lines 62-63), said method comprising steps of: detecting power shutdown (page 2, column 4, lines 27-30); and changing the high speed operation mode to the low speed operation mode (page 2, column 3, lines 36-39). Bui fails to disclose determining whether the power shutdown is recovered within a given period; and setting the high speed operation mode when the power shutdown is determined to be recovered. Arai teaches a method for controlling a microcomputer system that functions in a high speed operation mode and a low speed operation mode (page 3, column 5, lines 28-30) with a backup power supply (page 2, column 3, lines 58-59), said method

comprising steps of detecting power shutdown (page 3, column 6, lines 31-32), similar to Bui. Arai teaches the method further comprising determining whether the power shutdown is recovered within a given time period (page 2, column 3, lines 31-33); and setting the high speed operation mode when the power shutdown is determined to be recovered (page 2, column 3, lines 33-37) so that "[t]he last operating conditions of the computer system can be resumed within a short time" (page 2, column 3, lines 33-35). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art, having references Bui and Arai in front of them, to combine the disclosure of Bui's variable clock speed system with the teachings of Arai's speed control and power resumption. The motivation for doing so would have been for an expedient recovery of the last operating conditions of the system.

6. With respect to claim 2, Arai further teaches the method for controlling a microcomputer according to claim 1 wherein the clock measures the given time period in the low speed operation mode (page 4, column 7, line 44-45).

7. With respect to claim 3, Arai further teaches the method for controlling a microcomputer according to claim 1, further comprising a step of setting the microcomputer to a stop operation mode to stop operations unless the power shutdown is recovered within the given time period (page 4, column 7, lines 58-61).

8. With respect to claim 6, though Arai does not expressly teach that the second given time period is set to be longer than the first given time period by substantially an integral multiple. However, due to the finite precision of the clock frequency upon which the first given time period is dependent, the second given time period would necessarily

have to be set to substantially an integral multiple greater than the first given time period.

9. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui (U.S. 6,763,478) in view of Arai (5,978,922), and in further view of Klein (U.S. 6,178,523).

10. With respect to claim 5, Bui discloses a method for controlling a microcomputer in a microcomputer system (page 2, column 3, lines 60-61) with a high speed operation mode and a low speed operation mode (page 2, column 3, lines 60-64) in which operations of the microcomputer are slower than that of the high speed operation mode, said microcomputer system including a clock operable in the high and the low speed operation mode (page 2, column 4, lines 65-67 and page 3, column 5, lines 1-2) and a backup power supply for supplying the clock with power for a predetermined time (page 2, column 3, lines 62-63), said method comprising steps of: detecting power shutdown (page 2, column 4, lines 27-30); and changing the high speed operation mode to the low speed operation mode (page 2, column 3, lines 36-39). Bui does not disclose periodically determining whether the power shutdown is recovered within a first given time period. Bui also fails to disclose setting the high speed operation mode when the power shutdown is determined to be recovered; and setting the microcomputer to a stop operation mode to stop operations unless the power shutdown is recovered within the second given time period which is longer than the first given time period. Arai teaches a method for controlling a microcomputer system that functions in a high speed operation mode and a low speed operation mode (page 3, column 5, lines 28-30) with a backup

power supply (page 2, column 3, lines 58-59), said method comprising steps of detecting power shutdown (page 3, column 6, lines 31-32), similar to Bui. Arai teaches the method further comprising determining whether the power shutdown is recovered within a given first time period (page 2, column 3, lines 31-33); setting the high speed operation mode when the power shutdown is determined to be recovered (page 2, column 3, lines 33-37); and setting the microcomputer to a stop operation mode to stop operation unless the power shutdown is recovered within the second given time period (page 4, column 7, lines 58-61). Arai does not teach periodically determining whether the power shutdown has recovered within a first given time period. Klein teaches a method for controlling a microcomputer system that functions in a high speed operation mode and low speed operation mode, with a backup power supply, similar to Bui and Arai. Klein teaches the method further comprising periodically determining whether the power shutdown is recovered within a first given time period (page 3, column 6, lines 5-13) in order to conserve power by determining the earliest point of possible power shutdown recovery. Arai does not expressly teach that the second time period is longer than the first given time period. However, in order for Arai's method to perform properly, the second time period would have to necessarily be longer than the given first time period determined by the frequency of the clock in low speed operation mode in order to properly detect shutdown recovery. At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the disclosure of Bui's variable clock speed system with the teachings of Arai's speed control and power resumption and Klein's periodic recovery checking. The motivation for doing so would have been

for an expedient recovery of the last operating conditions of the system and to determine the earliest possible point at which the high speed operation mode could be restored, saving time and the life of the backup power supply.

11. With respect to claim 8, Bui discloses a method for controlling a microcomputer in a microcomputer system (page 2, column 3, lines 60-61) with a high speed operation mode and a low speed operation mode (page 2, column 3, lines 60-64) in which operations of the microcomputer are slower than that of the high speed operation mode, said microcomputer system including a clock operable in the high and the low speed operation mode (page 2, column 4, lines 65-67 and page 3, column 5, lines 1-2) and a backup power supply for supplying the clock with power for a predetermined time (page 2, column 3, lines 62-63), said method comprising steps of: detecting power shutdown (page 2, column 4, lines 27-30); and changing the high speed operation mode to the low speed operation mode when the clock is set (page 2, column 3, lines 36-39). Bui does not disclose checking whether the clock is set or setting the microcomputer to a stop operation mode to stop operations unless the clock is set. However, it would have been obvious to one skilled in the art at the time of the invention that if the clock were not set, the microcomputer would have to be set to a stop operation mode since it would not be available to operate in either the low or high speed operation modes. Bui fails to disclose periodically determining whether the power shutdown is recovered within a first given time period. Bui also does not disclose setting the high speed operation mode when the power shutdown is determined to be recovered; and setting the microcomputer to the stop operation mode to stop operations unless the power

shutdown is recovered within the second given time period which is longer than the first given time period. Arai teaches a method for controlling a microcomputer system that functions in a high speed operation mode and a low speed operation mode (page 3, column 5, lines 28-30) with a backup power supply (page 2, column 3, lines 58-59), said method comprising steps of detecting power shutdown (page 3, column 6, lines 31-32), similar to Bui. Arai teaches the method further comprising determining whether the power shutdown is recovered within a given first time period (page 2, column 3, lines 31-33); setting the high speed operation mode when the power shutdown is determined to be recovered (page 2, column 3, lines 33-37); and setting the microcomputer to a stop operation mode to stop operation unless the power shutdown is recovered within the second given time period (page 4, column 7, lines 58-61). Arai does not teach periodically determining whether the power shutdown has recovered within a first given time period. Klein teaches a method for controlling a microcomputer system that functions in a high speed operation mode and low speed operation mode, with a backup power supply, similar to Bui and Arai. Klein teaches the method further comprising periodically determining whether the power shutdown is recovered within a first given time period (page 3, column 6, lines 5-13) in order to conserve power by determining the earliest point of possible power shutdown recovery. Arai does not expressly teach that the second time period be longer than the first given time period. However, in order for Arai's method to perform properly, the second time period would have to necessarily be longer than the given first time period determined by the frequency of the clock in low speed operation mode in order to properly detect shutdown recovery. At the time of the

invention it would have been obvious to a person of ordinary skill in the art to combine the disclosure of Bui's variable clock speed system with the teachings of Arai's speed control and power resumption. The motivation for doing so would have been for an expedient recovery of the last operating conditions of the system and to determine the earliest possible point at which the high speed operation mode could be restored, saving time and the life of the backup power supply.

12. Claims 4, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui (U.S. 6,763,478) in view of Kohn (The IEEE Standard Dictionary of Electrical and Electronics Terms, 6th ed.) and Arai (5,978,922).

13. With respect to claim 4, Arai further teaches the method for controlling a microcomputer according to claim 1, wherein the microcomputer measures a time period during power shutdown (page 4, column 7, lines 58-61). Arai fails to explicitly teach storing the value representing said time period in volatile memory. However, it is well known in the art that counters are used to store values representing time periods. Kohn defines a counter as "A device such as a register or storage location used to represent the number of occurrences of an event" (page 228). As registers are a type of volatile memory, the value representing the time period would necessarily have to be stored in volatile memory.

14. With respect to claim 7, Arai further teaches the method for controlling a microcomputer according to claim 5, wherein the microcomputer measures a time period during power shutdown (page 4, column 7, lines 58-61). Arai fails to explicitly teach storing the value representing said time period in volatile memory. However, it is

well known in the art that counters are used to store values representing time periods. Kohn defines a counter as "A device such as a register or storage location used to represent the number of occurrences of an event" (page 228). As registers are a type of volatile memory, the value representing the time period would necessarily have to be stored in volatile memory.

15. With respect to claim 9, Arai further teaches the method for controlling a microcomputer according to claim 8, wherein the microcomputer measures a time period during power shutdown (page 4, column 7, lines 58-61). Arai fails to explicitly teach storing the value representing said time period in volatile memory. However, it is well known in the art that counters are used to store values representing time periods. Kohn defines a counter as "A device such as a register or storage location used to represent the number of occurrences of an event" (page 228). As registers are a type of volatile memory, the value representing the time period would necessarily have to be stored in volatile memory.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Novoa (U.S. 5,925,131), Lacombe (U.S. 6,026,495), and Reitweisner (U.S. 5,485,363).

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward K. Park whose telephone number is (571) 272-5859. The examiner can normally be reached on M-F, 8:30 AM - 5:00 PM.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ekp

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~3600~~ 2100